In ~~T~~the Specification:

Page 2, line 1 to the third paragraph.

gate electrode 16 is constructed by a metal layer or a polysilicon layer 20 and an underlayer, a gate oxide layer 18. In order to describe or simulate~~apply~~ the operation of the MOS on the computer ~~to simulate it's operation condition more easily~~, the structure of the MOS is represented by~~simplify into~~ circuit symbols. Fig. 1B is a circuit symbol ~~model~~ of a conventional NMOS transistor.

Figs. 1C and 1D are ~~character~~ diagrams showing characteristics of the NMOS transistor. Since the source and the substrate of the NMOS are usually grounded, ~~performance~~operation of the NMOS is controlled by the Vg and the Vd, wherein the Vg decides the switch state (on/off state) of the NMOS and the Vd decides the amount of the current passing through the drain, channel and source when the NMOS is opened. Therefore, as shown in Fig. 1C, the current Id in the NMOS is almost zero when Vg is smaller than Vt. Simultaneously, when Vg is larger than Vt, the current Id in the NMOS is proportionally increased with the Vg. As shown in Fig. 1D, under Vg1, Vg2 and Vg3 (while Vg1<Vg2<Vg3), Id is directly proportional to Vd when Vd is relatively small. When the Vd is increased to reach a saturated drain voltage, the Id is approaching~~closing~~ to a~~n~~ saturated situation.

~~Basing~~Based on the characteristics~~factors~~ provided by the ~~character~~ curves in Figs. 1C and 1D, various circuit characters of the NMOS shown in Fig. 1B can be simulated by the computer.

Page 4, line 18-page 5, line 6

Fig. 1A is schematic, cross-sectional view of a conventional N-type MOS transistor;

Fig. 1B is a circuit symbol ~~model~~ of a conventional NMOS transistor;

 BEST AVAILABLE COPY

PAGE 3/8 * RCVD AT 8/6/2004 6:20:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:19496600809 * DURATION (mm-ss):02-40

Figs. 1C and 1D are ~~character~~ diagrams showing characteristics of the NMOS transistor;

Fig. 2 is schematic, cross-sectional view of an NROM structure to be ~~for being~~ modeled in a preferred embodiment according to the invention;

Fig. 3 is schematic view of~~,~~ a macro model of an NROM structure in a preferred embodiment according to the invention;

Fig. 4A, a plot of I_D versus V_G, ~~is~~shows a character curve~~diagram~~ of an NROM structure under the forward reading operation mode;

Fig. 4B is a schematic view of an NROM structure under a forward reading~~bias~~ operation mode;

Fig. 5A, a plot of I_D versus V_G, ~~is~~shows a character curve~~diagram~~ of an NROM structure under the reverse reading operation mode; and

Fig. 5B is a schematic view of an NROM structure under a reverse reading~~bias~~ operation mode.

Page 6, the second paragraph to page 7, line 2.

Fig. 3 is schematic~~,~~ view of a macro model of an NROM structure in a preferred embodiment according to the invention. As shown in Fig. 3, since the left-hand part of the NROM shown in Fig. 2 is a normal NMOS structure and the right-hand part of the NROM is an NMOS transistor with short channel length, high threshold voltage and serious DIBL effect because of the existence of charge trapped region 46, a normal MOS symbol element 50 in serial~~series~~ with a short channel MOS symbol element 52 is used to represented the NROM structure described

BEST AVAILABLE COPY

PAGE 4/8 * RCVD AT 8/6/2004 6:20:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:19496600809 * DURATION (mm-ss):02-40

above. It should be noticed that a MOS possesses the channel shorter than the channel of the MOS symbol element 50 is regarded as a short channel MOS. In Fig. 3~~eidentaly~~, the normal MOS symbol element 50 comprising a first gate electrode 54, a first drain 56 and a first source 58 represents a MOS constructed by the drain 32, the source 34 and the left portion of the gate electrode 36 without the existence of charge trapped region 46. Moreover, the short channel MOS symbol element 52 comprising a second gate electrode 60, a second drain 64 and a second source 62 represents a MOS constructed by the drain 32, the source 34 and the other portion of the gate electrode 36 with the charge trapped region 46.

Furthermore, since the normal MOS symbol element 50 and the short channel MOS symbol element 52 share a common gate electrode as the gate electrode 36 shown in Fig. 2, the first gate electrode 54 is coupled with the second gate electrode 60. In addition, by comparing Fig. 2 to Fig. 3, since the first drain 56 is, indeed, the second source 62 ~~so that~~ the first drain 56 is in series coupled with the second source 62.

Page 8, last paragraph to page 9, line 8.

As shown in Fig. 5B~~A~~, when the NROM is operated under a reverse bias, charges are stored close to the source 34. The applied voltage V_D at drain will not affect the performance of the short channel MOS symbol element 90 unless the normal MOS symbol element 92 is "on"~~so seriously as under forward reading operation because the negative charges are stored close to the source 34~~. Clearly, both normal MOS symbol element 92 and short channel MOS symbol element 90 could affect the performance of the NROM. Therefore, only when a high voltage V_G is applied on the

BEST AVAILABLE COPY

PAGE 5/8 * RCVD AT 8/6/2004 6:20:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:19496600809 * DURATION (mm-ss):02-40

gate electrode even ~~though V_D is high~~ (as represented by curve 82 in Fig. 5A, V_D=2.1V), the normal MOS symbol element 92 and the short channel MOS symbol element 90 are turned on at the same time~~. Therefore, the~~ to generate a larger I_D ~~is relatively large~~. If the applied voltage V_D is as low as the applied voltage V_D (V_D=0.1V) used in the forward bias operation mode, a relatively high V_G (as shown by curve 80 in Fig. 5A, larger than 2.1V) is necessary for inducing relatively large current I_D.

BEST AVAILABLE COPY

PAGE 6/8 * RCVD AT 8/6/2004 6:20:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:19496600809 * DURATION (mm-ss):02-40